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Single-Phase Common-Ground-Type Transformerless PV Grid-Connected Inverters

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ABSTRACT This paper presents a family of novel common-ground-type transformerless photovoltaic (PV) grid-connected inverters, which requires only five power switches, one capacitor, and one filter. A simple dual-closed led-loop control is used to improve control stabilization and accuracy. The main advantages of proposed inverters are: 1) the leakage current is completely eliminated (unlike traditional topologies, which can only suppress leakage current); 2) the devices used are a few and the cost is low; 3) low loss and high efficiency; 4) the ability of realizing reactive power; and 5) there is no need for high DC input voltage compared with half-bridge-type topologies. The operating principle, modulation mode, and control strategy are introduced in detail. The performance of the proposed topology is compared with that of several traditional topologies. The leakage current suppression ability and efficiency of the proposed topology are superior to those of the traditional topologies. The model predictive control (MPC) is applied in the proposed topology, which is easy to realize and can accelerate the dynamic response. Finally, the simulation and experimental results of a 1-kVA prototype are given, which proves the validity of the proposed topology in PV grid-connected system.

INDEX TERMS Photovoltaic power generation, transformerless, grid-connected inverter, leakage current, model predictive control.

I. INTRODUCTION

Transformerless PV grid-connected inverters have the advantages of small volume, light weight, low cost and high efficiency. However, removing the transformer leads to electrical connection between PV panels and utility grid, resulting in common mode (CM) leakage current, which increases grid-connected current harmonics, system losses, and even causes safety issues [1], [2]. Therefore, the application of transformerless PV inverters must meet strict safety standards [3]. In recent years, with increasing application of transformerless PV grid-connected inverters, the research of new topologies to suppress leakage current has become a subject of interest in PV grid-connected systems.

The half-bridge-type inverters connect the utility grid neutral point to the midpoint of DC-link capacitors, so the voltage on parasitic capacitor of PV panels remains unchanged, and the leakage current can be suppressed [4]. However, half-bridge-type inverters require a large DC input voltage, which is about twice that of full-bridge-type inverters. The DC- side voltage utilization is low [5], [6]. The single-phase full-bridge topology with bipolar sinusoidal pulse width modulation (SPWM) also has the ability to suppress leakage current, but its two-level output voltage makes the grid-connected current harmonic larger, which requires a large filter inductor [7]. Topologies most widely used are H5 topology proposed in [8], HERIC topology proposed in [9] and the corresponding improved topologies proposed in [10]–[13]. This type of topology suppresses leakage current by DC/AC decoupling. However, due to the existence of switch junction capacitors, this kind of method cannot completely disconnect the circuit, so there is still leakage current [14]. Although leakage current can be better suppressed by adding neutral point clamp (NPC) structure. It cannot be eliminated completely, and loss and cost will be increased because of extra structure [15].

The common-ground topology is a kind of topology proposed in recent years, which can completely eliminate

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leakage current. The principle is to directly connect the negative terminal of PV panels to neutral point of the utility grid, which is equivalent to short-circuiting the parasitic capacitor of PV panels. A common-ground topology based on virtual DC bus structure is proposed in [16]. However, the flying capacitor is not charged in negative half cycle, so the output voltage is distorted in negative half period. The topology proposed in [17] has a two-level output voltage, which has high harmonic content. A multilevel common-ground topology is proposed in [18]. But the control method of this topology is very complex. The more the level number, the more complex the control is, so it is difficult to realize in practical application. A common-ground topology similar to the virtual DC bus is also proposed in [19]. However, it requires two-stage energy transmission, which increases the loss. Some of the single-phase common-ground transformerless inverters are shown in Fig. 1.

In view of the above shortcomings, this paper proposes a flying capacitor charging and discharging structure. Then a new family of transformerless PV grid-connected topologies are derived based on this structure. The topology directly connects the neutral point of utility grid to negative terminal of PV panels, and the leakage current can be eliminated completely. In addition, the topology requires only 5 switches, which reduces the cost of semiconductor devices. During the operation of inverter, the current only flows through two switches, reducing conduction losses. Under the same parameters, the performance of H5, HERIC and proposed topology are compared and analyzed by PSIM, and their efficiencies are compared through loss calculations. Finally, a 1kVA prototype is built to verify the correctness and good performance of proposed topology.

II. PROPOSED TOPOLOGIES AND PRINCIPLES OF OPERATION

A. PROPOSAL OF NEW TOPOLOGY

The proposed flying capacitor charge-discharge structure is shown in Fig. 2. When S_1 and S_4 are turned on, the flying capacitor C_{FC} is connected to the DC side and charged to the input voltage; when S_2 and S_3 are turned on, the capacitor generates negative voltage which is equal to the input voltage. This process continues to be repeated at switching frequency to maintain a constant output voltage. The neutral point of the utility grid is directly connected to the negative terminal of the PV panels, which is equivalent to short-circuiting the parasitic capacitor of PV panels. Therefore, the leakage current can be effectively eliminated.

Based on the flying capacitor charge-discharge structure, a family of novel topologies are derived, including five switches, two capacitors and one filter inductor, as shown in Fig. 3.

B. ANALYSIS OF WORKING MODE

Germany updated the standard of grid-connected inverter in 2011, which proposes the ability to realize reactive power for PV systems [20]. Traditional H5 and HERIC topology

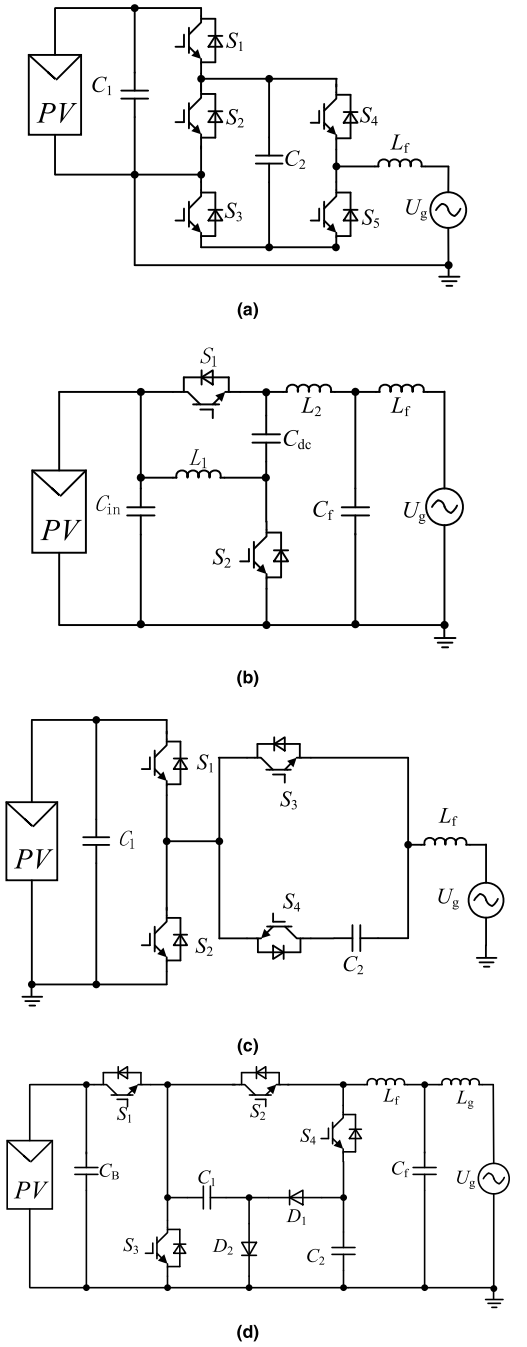

FIGURE 1. Single-phase common-ground transformerless inverters. (a) Topology proposed in [16]. (b) Topology proposed in [17]. (c) Topology proposed in [18]. (d) Topology proposed in [19].

do not have the ability to transmit reactive power. In order to meet the requirement in the standard, this paper proposes a modulation method, as shown in Fig. 4. Taking the first topology as an example, the working mode is analyzed in detail, and the other topologies are similar to it. According to the direction of grid-connected current and grid voltage, the working mode can be divided into four intervals. Each interval has two stages.

Interval I: $i_g > 0$, $U_g > 0$. In stage 1, energy is transferred from dc side to grid side, as shown in Fig. 5(a). In stage 1,

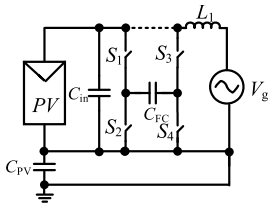

FIGURE 2. Flying capacitor charge-discharge structure.

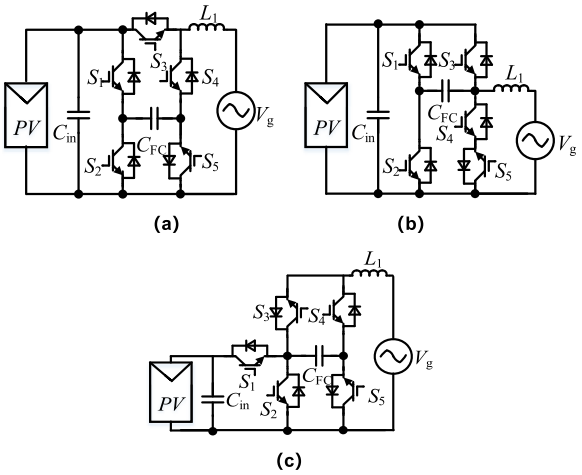

FIGURE 3. Proposed topologies. (a) Novel topology I, (b) Novel topology II, and (c) Novel topology III.

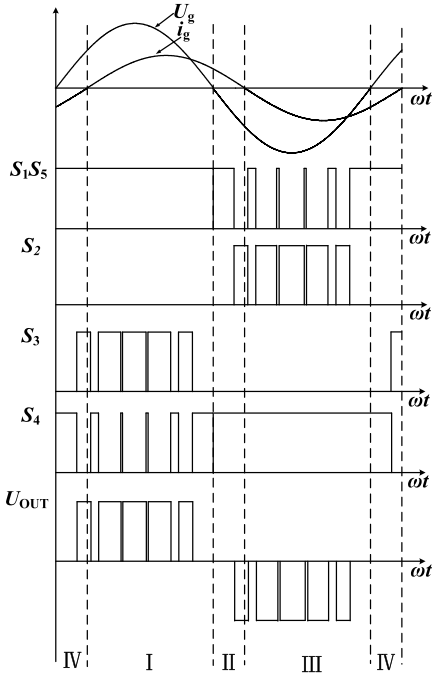

FIGURE 4. Modulation mode.

PV panels charge the inductor through S_3; In stage 2, the inductor discharges through S_4 and S_5. PV panels charge the flying capacitor C_{FC} through S_1 and S_5 over the entire interval.

Interval II: $i_g > 0$, $U_g < 0$. In stage 1, energy is transferred from grid side to dc side, as shown in Fig. 5(b). In stage 1, the grid charges the flying capacitor and inductor through S_2 and S_4. In stage 2, the current flows through S_5, S_4, L_1 and the grid.

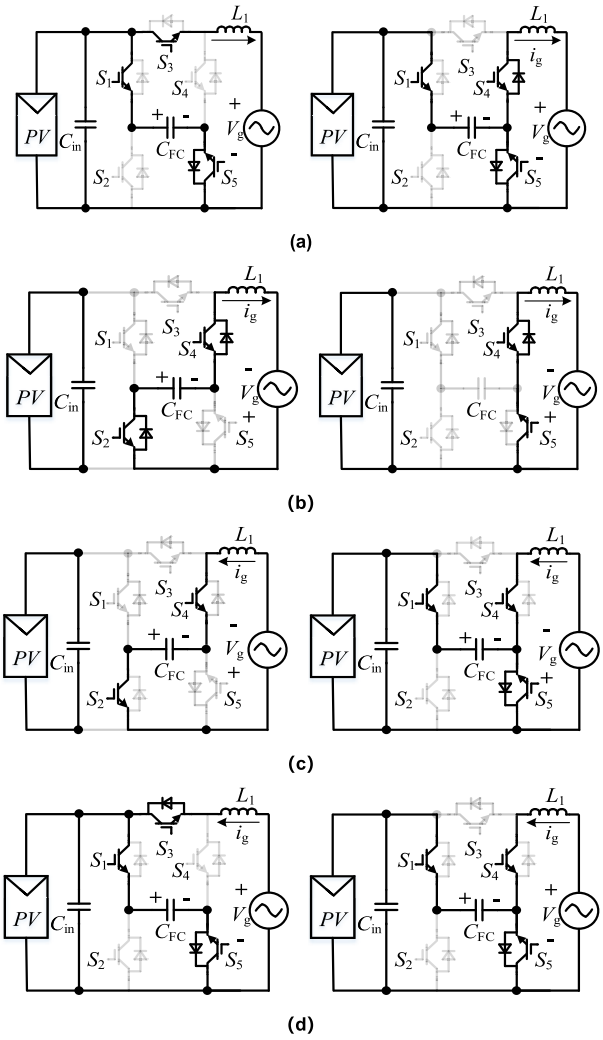

FIGURE 5. Working modes. (a) Interval I. (b) Interval II. (c) Interval III. (d) Interval IV.

Interval III: $i_g < 0$, $U_g < 0$. In stage 1, energy is transferred from flying capacitor to grid through S_4, as shown in Fig. 5(c). In stage 2, the inductor discharges through S_4 and S_5 and PV panels charge the flying capacitor C_{FC} through S_1 and S_5.

Interval IV: $i_g < 0$, $U_g > 0$. In stage 1, energy is transferred from grid side to dc side, as shown in Fig. 5(d). The grid charges the flying capacitor and inductor through S_1, S_3 and S_5. In stage 2, PV panels charge the flying capacitor C_{FC}. Over the entire interval, PV panels charge the flying capacitor C_{FC} through S_1 and S_5.

If the PV system operates at a unit power factor, it will circle in the order of I-II-I-III. If it is required to transmit reactive power in the PV system, it will circle in the order of I-II-III-IV or I-IV-III-II.

C. FLYING CAPACITOR SELECTION

The main idea of proposed topology is to charge the flying capacitor at the positive half period of grid voltage and to

supply the power by the flying capacitor at the negative half period. Therefore, the choice of flying capacitor is very important for proposed topology.

During a switching cycle, there are three modes of flying capacitor charging and one mode of discharging. The energy released by the capacitor is approximately equal to the energy absorbed by the unity grid. A model can be built, as shown in (1).

$$\frac{1}{2}C(u_1^2 - u_2^2) = \int_{t_1}^{t_1+\Delta t} u_g i_g dt$$
$$t_1 \in (0.01 + 0.02k, 0.02 + 0.02k), \quad k \in N \tag{1}$$

where u_1 and u_2 are voltage of flying capacitor, u_g and i_g are the voltage and current of the unity grid.

$$u_g = U_g \sin(\omega t) \tag{2}$$
$$i_g = I_g \sin(\omega t) \tag{3}$$
$$\Delta t = \frac{1}{4} \times \frac{1}{f_{sw}} \tag{4}$$

The energy absorbed by the unity grid is:

$$\int_{t_1}^{t_1+\Delta t} U_g I_g \sin^2(\omega t) dt$$
$$= \frac{1}{2} U_g I_g \int_{t_1}^{t_1+\Delta t} (1 - \cos 2\omega t) dt$$
$$= (\frac{1}{2}\Delta t - \frac{1}{4\omega}(\sin 2\omega(t_1 + \Delta t) - \sin 2\omega t_1)) U_g I_g \tag{5}$$

Substituting (5) to (1), the formula (1) can be simplified to:

$$C = \frac{(\Delta t - \frac{1}{2\omega}(\sin 2\omega(t_1 + \Delta t) - \sin 2\omega t_1)) U_g I_g}{(u_1^2 - u_2^2)} \tag{6}$$

By using the knowledge of integral transformation, the maximum value of (6) can be obtained when $t_1 = t^* = 0.015$.

$$C_{\max} = \frac{(\Delta t - \frac{1}{2\omega}(\sin 2\omega(t^* + \Delta t) - \sin 2\omega t^*)) U_g I_g}{(u_1^2 - u_2^2)} \tag{7}$$

This article parameter is set to:

$$U_g = 220\sqrt{2}\text{V}, \quad I_g = 5\text{A}, f_{sw} = 20\text{kHz},$$
$$\omega = 2\pi f = 100\pi, \quad u_1 = 400V_{\circ}$$

Substituting data to (7):

$$C_{\max} = \frac{(\Delta t - \frac{1}{2\omega}(\sin 2\omega(t^* + \Delta t) - \sin 2\omega t^*)) U_g I_g}{(u_1^2 - u_2^2)}$$
$$= \frac{0.03889}{400^2 - u_2^2} \tag{8}$$

From (8), the value of the flying capacitor is related to u_2. The larger the flying capacitor is, the smaller the voltage changes, but the cost is higher; the smaller the flying capacitor is, the lower the cost is, but the voltage varies greatly and the output voltage is distorted. A large discharge current is generated, resulting in a large equivalent series resistance (ESR) loss of capacitor. u_2 is chose to be 399.9V under the comprehensive consideration, which only has 0.1V change and has little effect on the output voltage. So, the value of flying capacitor is 486uF. The capacitor of 470uF/600v is chosen under practical applications in this paper.

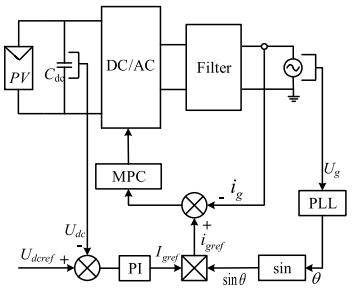

FIGURE 6. Control system.

III. CONTROL SYSTEM

Fig. 6 shows the control system of single-phase transformerless PV grid-connected inverter. The whole system consists of two closed loops: voltage outer loop and current inner loop. The voltage outer loop samples the unity grid voltage and detects the phase and frequency through the phase-locked loop (PLL) to provide the current reference signal with the same frequency and phase as the grid voltage. The current inner loop samples the grid-connected current and compare it with the given current to obtain the driving signal of the switches.

Traditional controller generally uses PI, PR or QPR control, as shown in (9) ∼ (11).

$$G_{pi(S)} = K_P + \frac{K_i}{s} \tag{9}$$
$$G_{pr(S)} = K_P + \frac{2K_R \text{s}}{\text{s}^2 + w_g^2} \tag{10}$$
$$G_{qpr(S)} = K_P + \frac{2K_R \omega_{\text{r}} \text{s}}{\text{s}^2 + 2\omega_{\text{r}} s + w_g^2} \tag{11}$$

The bode diagram of the three controllers is shown in Fig. 7. The PI controller does not have a large gain at grid frequency, so there is a steady state error. Although the PR controller provides a large gain at grid frequency, the gain at other frequency points is minimal, as shown in Fig. 7(a). Once the grid frequency is disturbed, the controller cannot track the sinusoidal signal quickly and accurately. The QPR controller broadens the bandwidth at grid frequency based on the PR controller, which can suppress the impact of the grid frequency fluctuation, but the gain will be greatly reduced, as shown in Fig. 7(b).

These three controllers have their own shortcomings. This paper uses model predictive control (MPC), which does not

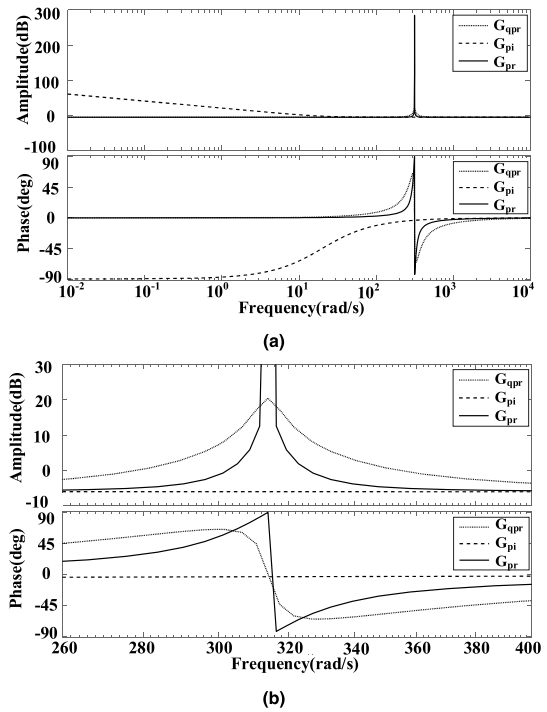

FIGURE 7. Bode diagram. (a) PI, PR, and QPR bode diagram. (b) Expanded diagram.

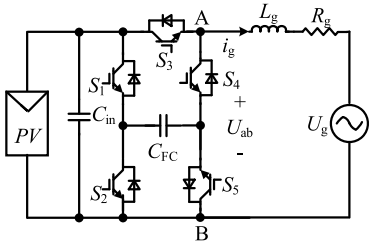

FIGURE 8. MPC model of the inverter topology.

need a PWM modulator and has the ability to accelerate dynamic response.

The MPC model is shown in Fig. 8. The mathematical model of filter inductor charging-discharging is established. The Kirchhof's voltage law (KVL) is applied to establish dynamic equation of grid-connected current, as shown in (12).

$$U_{\mathrm{ab}} - i_g \cdot R_g - U_g = L_g \frac{di_g}{dt} \tag{12}$$

where U_{ab} is output voltage, i_{g} is grid-connected current, R_{g} is equivalent resistor of circuit, U_{g} is the grid voltage.

As long as the sampling frequency f_{s} is large enough (the sampling period $\mathrm{T_s}$ is 100k in this paper), the forward Euler approach formula can be used to replace the grid-connected current derivative.

$$\frac{di_g}{dt} \approx \frac{i_g(k+1) - i_g(k)}{T_S} \tag{13}$$

TABLE 1. Working modes.

S_1	S_2	S_3	S_4	S_5	output voltage U_{ab}
1	0	1	0	1	U_{dc}
1	0	0	1	1	0
0	1	0	1	0	$-U_{\mathrm{dc}}$
1	0	0	1	1	0

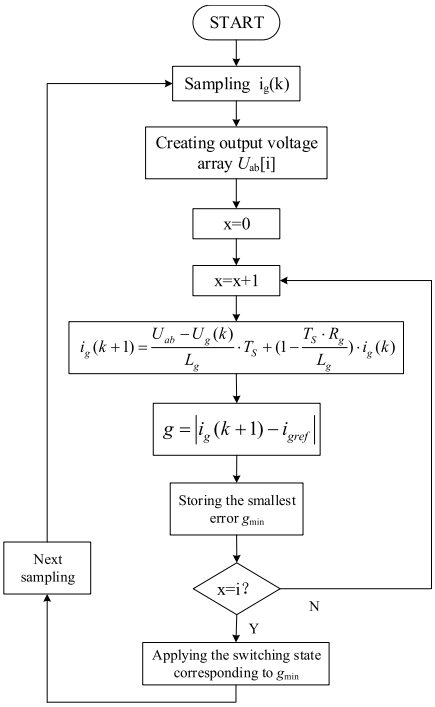

FIGURE 9. Flowchart of MPC.

Substituting (13) into (12), the MPC discrete model is obtained:

$$i_g(k+1) = \frac{U_{ab} - U_g(k)}{L_g} \cdot T_S + (1 - \frac{T_S \cdot R_g}{L_g}) \cdot i_g(k) \tag{14}$$

From (14), the predicted value of the grid-connected current at the next sampling time can be obtained from the variable value of the current sampling time. According to Table 1, there are four predictive grid-connected current corresponding four working modes.

The basic control goal of grid-connected inverter is to realize grid-connected current tracking given current, which means minimizing the error between the grid-connected current and the given current. According to (14), the grid-connected current of each working mode can be calculated and compared with the given current, and the error can be obtained.

The error is

$$g = \left| i_g(k+1) - i_{gref} \right| \tag{15}$$

Each error corresponds to a set of switching states, and the one with the least error is the optimal switching state. The working mode correspond to the least error is the next state. The flowchart of MPC is shown in Fig. 9.

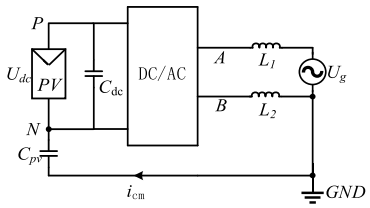

FIGURE 10. Leakage current equivalent model.

The MPC control does not need any modulators, which will have a quick dynamic response. Compared with PI or PR control, it does not need to set controller parameters, which is easy to realize. The MPC control can change cost function to optimize the performance of inverter.

IV. ANALYSIS OF LEAKAGE CURRENT ELIMINATION

A. LEAKAGE CURRENT EQUIVALENT MODEL

Fig. 10 shows the CM equivalent model of single-phase transformerless PV grid-connected inverter. $U_{\rm dc}$ is the input DC voltage; $C_{\rm pv}$ is the PV parasitic capacitor; $C_{\rm dc}$ is the voltage stabilizing capacitor; L_1 and L_2 are filter Inductors.

The total CM voltage U_{TCM} is defined as:

$$U_{TCM} = \frac{U_{AN} + U_{BN}}{2} + (U_{AN} - U_{BN})\frac{L_2 - L_1}{2(L_1 + L_2)} \quad (16)$$

where $U_{\rm AN}$ and $U_{\rm BN}$ are the voltages of point A and point B to point N.

The leakage current $i_{\rm CM}$ is defined as:

$$i_{CM} = C_{pv}\frac{dU_{TCM}}{dt} \quad (17)$$

From (17), the leakage current can be eliminated as long as the total CM voltage $U_{\rm TCM}$ has no variation.

B. COMMON-MODE BEHAVIOR

The main method based on full-bridge improved topologies (such as H5 and HERIC) is to insert additional switches into traditional full-bridge inverter to decouple the DC side from the AC side. Then the CM voltage can be kept constant to suppress leakage current. However, in practical applications, this kind of decoupling is incomplete due to the exist of parasitic capacitors of switches. In the two modes of half period, the parasitic capacitors will be charged and discharged, which will affect the CM voltage. There will still be leakage currents.

Taking H5 topology as an example, in the positive half period, the working mode considering the parasitic capacitor of switches is shown in Fig. 11(a) and Fig. 11(b). In the power transmission mode, according to the equivalent circuit shown in Fig. 11(c):

$$U_{\rm AN} = U_{\rm DC} \quad (18)$$

$$U_{\rm BN} = 0 \quad (19)$$

The CM voltage is:

$$U_{CM} = \frac{U_{AN} + U_{BN}}{2} = \frac{U_{DC} + 0}{2} = \frac{U_{DC}}{2} \quad (20)$$

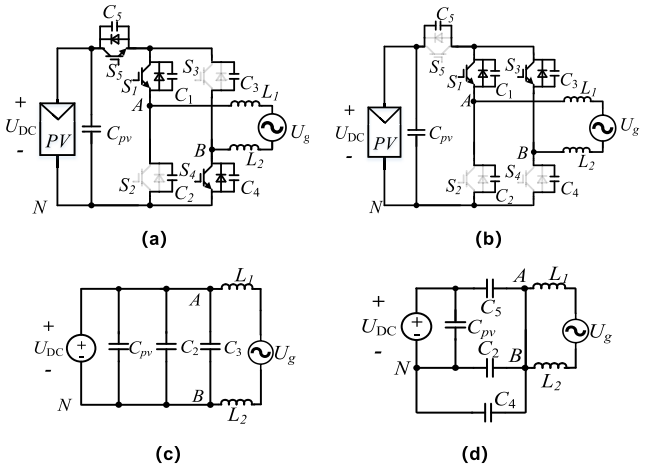

FIGURE 11. Positive half cycle mode of H5. (a) Mode 1 of H5. (b) Mode 2 of H5. (c) Mode 1 equivalent circuit. (d) Mode 2 equivalent circuit.

In the freewheeling mode, according to the equivalent circuit shown in Fig. 11(d), there is:

$$U_{AN} = U_{BN} = U_{DC} \cdot \frac{C_5}{C_2 + C_4 + C_5} \quad (21)$$

The CM voltage is:

$$U_{CM} = \frac{U_{AN} + U_{BN}}{2} = U_{DC} \cdot \frac{C_5}{C_2 + C_4 + C_5} \quad (22)$$

Choosing the same type of switches, it can be approximated that the parasitic capacitors of the switches are equal, $C_2 = C_4 = C_5$, then the CM voltage is:

$$U_{CM} = \frac{U_{DC}}{3} \quad (23)$$

It can be seen from (20) and (23) that the CM voltage $U_{\rm CM}$ cannot maintain as a constant in the power transmission mode and freewheeling mode, so H5 topology cannot completely eliminate the leakage current.

In the positive half period, the working mode considering the parasitic capacitors of switches of proposed topology is shown in Fig. 12(a) and Fig. 12(b). In the power transmission mode, according to the equivalent circuit shown in Fig. 12(c), there are:

$$U_{\rm AN} = U_{\rm DC} \quad (24)$$

$$U_{\rm BN} = 0 \quad (25)$$

The CM voltage is:

$$U_{CM} = \frac{U_{AN} + U_{BN}}{2} + (U_{AN} - U_{BN})\frac{L_2 - L_1}{2(L_1 + L_2)} = \frac{U_{DC}}{2} - \frac{U_{DC}}{2} = 0 \quad (26)$$

In the freewheeling mode, according to the equivalent circuit shown in Fig. 12(d), there is:

$$U_{\rm AN} = U_{\rm BN} = 0 \quad (27)$$

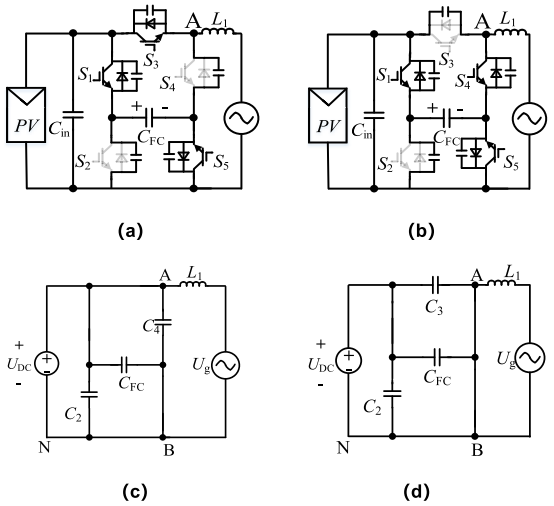

FIGURE 12. Positive half cycle mode of proposed topology. (a) Mode 1 of proposed topology. (b) Mode 2 of proposed topology. (c) Mode 1 equivalent circuit. (d) Mode 2 equivalent circuit.

TABLE 2. Comparison of device quantity.

Inverter	Switches	Diodes	Capacitors	Inductors
H5	5	0	1	2
HERIC	6	0	1	2
Hybird	6	2	1	2
Proposed	5	0	2	1

The CM voltage is:

$$U_{CM} = 0 \tag{28}$$

Therefore, when parasitic capacitor is considered, the CM voltage U_{CM} of proposed topology remains unchanged, and it has the ability to eliminate leakage current completely.

V. COMPARATIVE ANALYSIS

A. DEVICE COST COMPARISION

As shown in Table 2, the proposed topology only needs 5 switches, 2 capacitors and 1 inductor. The number of devices is similar to that of H5 topology, which is much less than that of other topologies, so it can save device cost and reduce the size of inverter.

B. LOSS CONTRAST ANALYSIS

In order to compare the efficiency of the proposed topology with other traditional topologies, this paper uses the same loss calculation method [21], [22] circuit parameters and devices to analyze the loss and efficiency of each topology. Under the same control strategy, DC input voltage, output voltage and switching frequency, the efficiency versus output power curve of the proposed topology, H5 topology and HERIC topology is shown in Fig. 13.

It can be seen from Fig. 13 that the proposed topology is more efficient than H5 topology and is similar to HERIC topology. Because of the presence of flying capacitor,

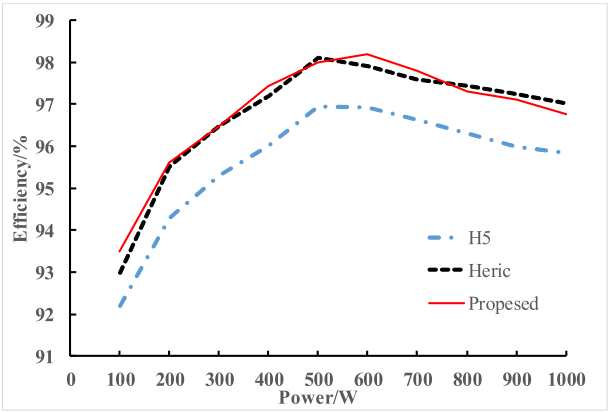

FIGURE 13. Efficiency contrast.

TABLE 3. Simulation and experiment parameters.

parameter	value
Input voltage	DC400V
Grid voltage	AC220V
Grid frequency	50Hz
Switching frequency	20kHz
Parasitic capacitor	75nF
Input capacitor	100μF
Filter inductor	4mH
ESR of inductor and circuit	0.6 Ω
Flying capacitor	470uF

the proposed inverter has a large ESR loss. The higher the power is, the greater ESR loss on the capacitor. Under the condition of low power application, the proposed topology is optimal. Under the condition of high power application, the HERIC topology is superior to the proposed topology.

C. SIMULATION RESULTS

In order to further verify the superiority of the proposed topology, the models of H5 topology, HERIC topology and proposed topology are built in simulator PSIM to verify the presented theoretical analysis. The simulation parameters are shown in Table 3.

Fig. 14 ∼ 16 show the simulation waveforms of the CM voltage and leakage current of the H5, HERIC and proposed topology. The CM voltage of H5 and HERIC topology fluctuates around 200V. Therefore, there is still leakage current, where the leakage current of HERIC topology is about 65mA and the leakage current of H5 topology is about 100mA, as shown in Fig. 14 and Fig. 15. The CM voltage of proposed topology is kept as a constant, so the leakage current is 0mA, as shown in Fig. 16.

Dynamic response of the inverter to step change in reference current of PR control and MPC control is shown in Fig. 17. In 0.111s, a step change is added in reference current. The grid-connected current in PR control takes about 50us to track the reference current, while the grid-connected current in MPC control takes only 5us, which

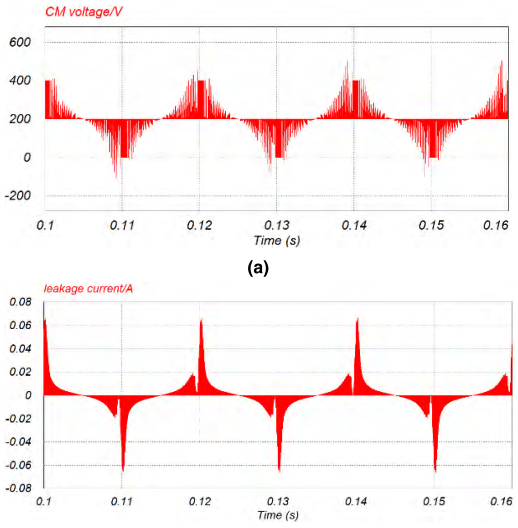

FIGURE 14. Simulation waveforms of HERIC topology. (a) CM voltage. (b) Leakage current.

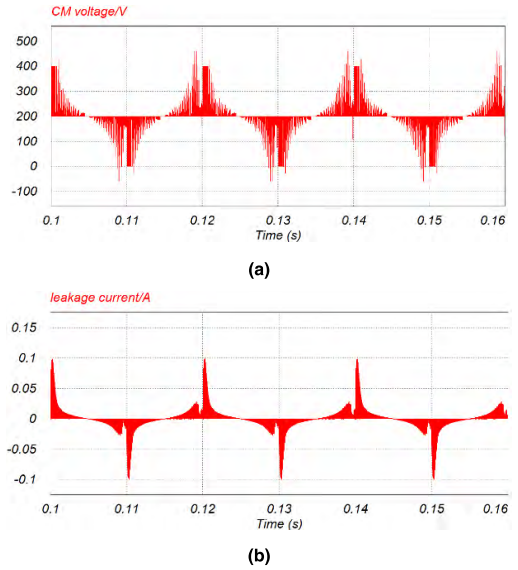

FIGURE 15. Simulation waveforms of H5 topology. (a) CM voltage. (b) Leakage current.

shows the advantage of quick dynamic response of MPC control. The THD of grid-connected current in QPR control is 2.1%, while the THD in MPC control is 1.9%, which does not have big difference. But the MPC control can change the cost function to reduce the THD.

D. EXPERIMENTAL RESULTS

A 1kVA prototype is designed to confirm the good performance of the proposed topology.

Fig. 18 shows the experiment prototype of the inverter. Fig. 19 shows the drive signals of switches. Fig. 20 shows the leakage current of proposed topology, the leakage current is about 20mA because of bypassing the parasitic capacitor of PV panels.

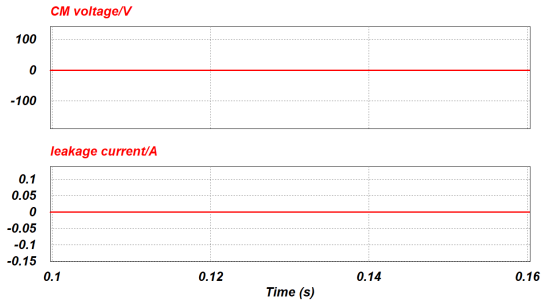

FIGURE 16. CM voltage and leakage current of proposed topology.

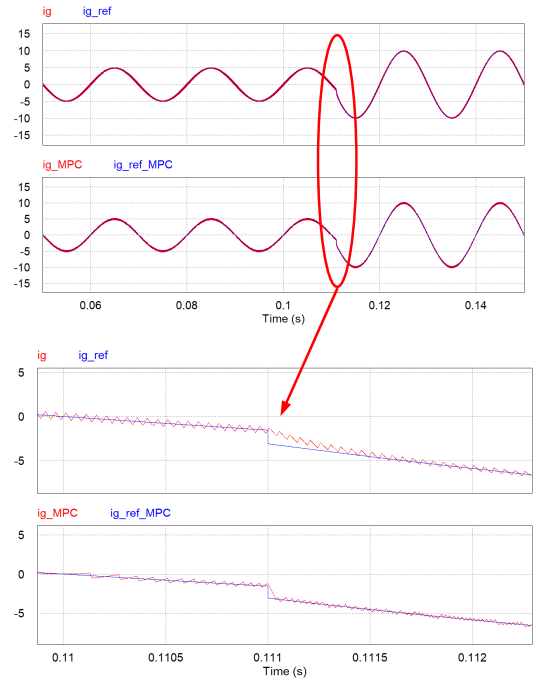

FIGURE 17. Comparison of simulation waveforms of grid-connect current and reference of current.

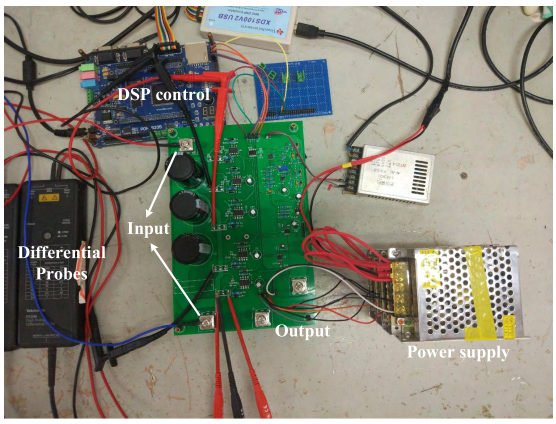

FIGURE 18. Experiment prototype.

Fig. 21 shows the experiment waveforms of output voltage U_{ab}, grid voltage U_g and flying capacitor voltage U_c. In the negative half period, because of the charging and

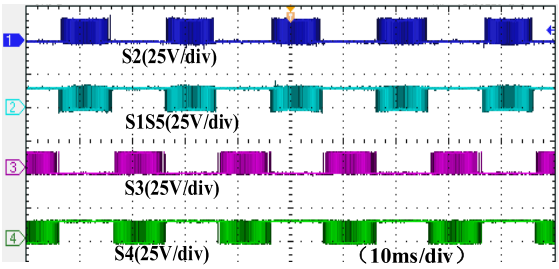

FIGURE 19. Experiment waveforms of switches drive signals.

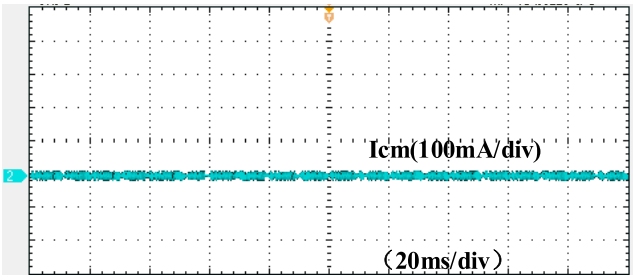

FIGURE 20. Experiment waveform of leakage current.

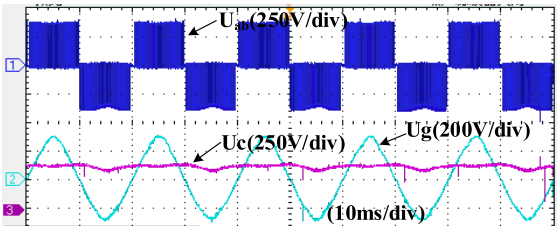

FIGURE 21. Experiment waveforms of output voltage U_{ab}, grid voltage U_g, and flying capacitor voltage U_c.

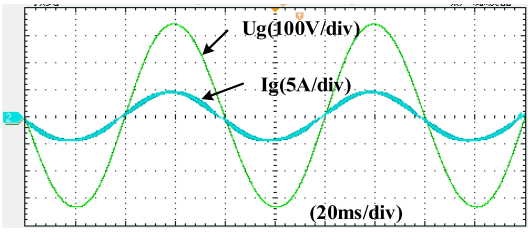

FIGURE 22. Experiment waveforms of grid voltage U_g and grid-connected current I_g under unit power factor.

discharging of flying capacitor, the output voltage U_{ab} has a little distortion, but has no influences to grid-connected current.

The experiment waveforms of grid voltage $U_g$and grid-connected current I_g under unit power factor are shown in Fig. 22. The current THD is 2.2%, which meets the requirement.

The experiment waveforms of grid voltage U_g and grid-connected current I_g under non-unit power factor are shown in Fig. 23, which verify the ability to adjust the reactive power of proposed topology.

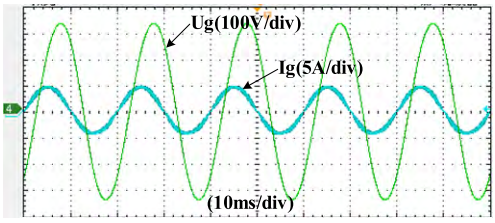

FIGURE 23. Experiment waveforms of grid voltage U_g and gridconnected current I_g under non-unit power factor.

VI. CONCLUSION

1) A family of common-ground-type transformerless PV grid-connected inverters and the MPC control strategy were introduced in this paper.

2) The negative terminal of PV panels is directly connected to neutral point of the utility grid, which can eliminate leakage current completely.

3) In order to meet the requirement in the new standard, this paper proposes a modulation method to adjust reactive power.

4) The proposed topologies need a minimum number of devices, which have a higher power density with lower design cost.

5) The proposed MPC control strategy does not need a PWM modulator, which is easy to realize and has the ability to accelerate dynamic response.

6) Simulations compare the proposed topology and other existing topologies, which shows the better performance of the proposed topology.

7) A 1kVA prototype of proposed topology is designed to confirm the correctness of theory and good performance of the proposed topology.

8) The proposed flying capacitor charge-discharge structure can be used to other common-ground topologies and provides a reference for new topologies.

APPENDIX

The proof of equation (16) is shown.

According to the definition of common-mode voltage and differential-mode voltage:

$$U_{CM} = \frac{U_{AN} + U_{BN}}{2} \tag{A-1}$$

$$U_{DM} = U_{AN} - U_{BN} \tag{A-2}$$

Replacing common-mode voltage and differential mode voltage with U_{AN} and U_{BN}:

$$U_{AN} = U_{CM} + \frac{U_{DM}}{2} \tag{A-3}$$

$$U_{BN} = U_{CM} - \frac{U_{DM}}{2} \tag{A-4}$$

Because the switching frequency is much higher than the grid frequency, the grid can be regarded as short circuit. Then Fig. 24 can be reduced to:

According to the Thevenin Theorem, the common-mode equivalent model shown in Fig. 25 can be simplified, and the simplest equivalent model can be obtained, as shown in Fig. 26.

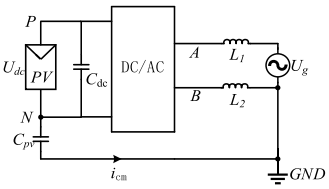

FIGURE 24. Leakage current common mode equivalent model.

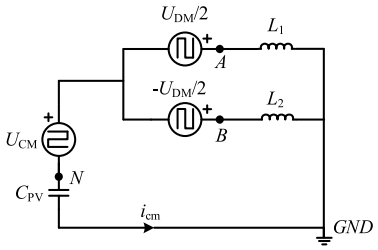

FIGURE 25. Common-mode equivalent model of single-phase transformerless PV grid-connected inverter.

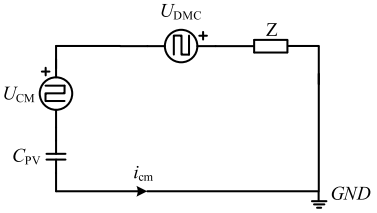

FIGURE 26. Simplest equivalent model.

where

$$U_{CM} = \frac{U_{AN} + U_{BN}}{2}, \quad U_{DMC} = (U_{AN} - U_{BN})\frac{L_2 - L_1}{2(L_1 + L_2)}.$$

The total common voltage is

$$\begin{aligned} U_{TCM} &= U_{CM} + U_{DMC} \\ &= \frac{U_{AN} + U_{BN}}{2} + (U_{AN} - U_{BN})\frac{L_2 - L_1}{2(L_1 + L_2)} \end{aligned} \quad \text{(A-5)}$$

REFERENCES

[1] H. Liu, Y. Ran, K. Liu, W. Wang, and D. Xu, "A modified single-phase transformerless Y-source PV grid-connected inverter," *IEEE Access*, vol. 6, pp. 18561–18569, 2018. doi: 10.1109/ACCESS.2018.2818188.

[2] H. López, J. Rodríguez-Reséndiz, X. Q. Guo, N. Vázquez, and R. V. Carrillo-Serrano, "Transformerless common-mode current-source inverter grid-connected for PV applications," *IEEE Access*, vol. 6, pp. 62944–62953, Oct. 2018. doi: 10.1109/ACCESS.2018.2873504.

[3] *Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid*, Standard DIN VDE V 0126-1-1, 2006.

[4] K. Kim, H. Cha, and H.-G. Kim, "A new single-phase switched-coupled-inductor DC–AC inverter for photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5016–5022, Jul. 2017. doi: 10.1109/TPEL.2016.2606489.

[5] Y. P. Siwakoti and F. Blaabjerg, "Common-ground-type transformerless inverters for single-phase solar photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2100–2111, Mar. 2018. doi: 10.1109/TIE.2017.2740821.

[6] B. Chen *et al.*, "A high-efficiency MOSFET transformerless inverter for nonisolated microinverter applications," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3610–3622, Jul. 2015. doi: 10.1109/TPEL.2014.2339320.

[7] T. K. S. Freddy, J.-H. Lee, H.-C. Moon, K.-B. Lee, and N. A. Rahim, "Modulation technique for single-phase transformerless photovoltaic inverters with reactive power capability," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 6989–6999, Sep. 2017. doi: 10.1109/TIE.2017.2686366.

[8] H. Li, Y. Zeng, B. Zhang, T. Q. Zheng, R. Hao, and Z. Yang, "An improved H5 topology with low common-mode current for transformerless PV grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1254–1265, Feb. 2019. doi: 10.1109/TPEL.2018.2833144.

[9] H. F. Xiao, K. Lan, and L. Zhang, "A quasi-unipolar SPWM full-bridge transformerless PV grid-connected inverter with constant common-mode voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3122–3132, Jun. 2015. doi: 10.1109/TPEL.2014.2331367.

[10] M. Islam and S. Mekhilef, "H6-type transformerless single-phase inverter for grid-tied photovoltaic system," *IET Power Electron.*, vol. 8, no. 4, pp. 636–644, 2015. doi: 10.1049/iet-pel.2014.0251.

[11] W. Cui, H. Luo, Y. Gu, W. Li, B. Yang, and X. He, "Hybrid-bridge transformerless photovoltaic grid-connected inverter," *IET Power Electron.*, vol. 8, no. 3, pp. 439–446, Mar. 2015. doi: 10.1049/iet-pel.2013.0785.

[12] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012. doi: 10.1109/TPEL.2011.2160359.

[13] L. Zhang, K. Sun, Y. Xing, and M. Xing, "H6 transformerless full-bridge PV grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1229–1238, Mar. 2014. doi: 10.1109/TPEL.2013.2260178.

[14] R. T. H. Li, C. N. M. Ho, and E.-X. Chen, "Active virtual ground—Single phase transformerless grid-connected voltage source inverter topology," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1335–1346, Feb. 2018. doi: 10.1109/TPEL.2017.2690146.

[15] J.-M. Shen, H.-L. Jou, and J.-C. Wu, "Novel transformerless grid-connected power converter with negative grounding for photovoltaic generation system," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1818–1829, Apr. 2012. doi: 10.1109/TPEL.2011.2170435.

[16] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793–805, Feb. 2013. doi: 10.1109/TPEL.2012.2203612.

[17] N. Vázquez, M. Rosas, C. Hernándezand, E. Vázquez, and F. J. Perez-Pinal, "A new common-mode transformerless photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6381–6391, Oct. 2015. doi: 10.1109/TIE.2015.2426146.

[18] A. Kadam and A. Shukla, "A multilevel transformerless inverter employing ground connection between PV negative terminal and grid neutral point," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8897–8907, Nov. 2017. doi: 10.1109/TIE.2017.2696460.

[19] J. F. Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei, and G. B. Gharehpetian, "A single-phase transformerless inverter with charge pump circuit concept for grid-tied PV applications," *IEEE Trans. Ind. Electron.*, vol. 46, no. 7, pp. 5403–5415, Jul. 2017. doi: 10.1109/TIE.2016.2645162.

[20] *Power Generation Systems Connected to the Low-Voltage Distribution Network—Technical Minimum Requirements for the Connection to and Parallel Operation With Low-Voltage Distribution Networks*, document VDE-AR-N 4105, 2011.

[21] X. Wang *et al.*, "Model predictive control methods of leakage current elimination for a three-level T-type transformerless PV inverter," *IET Power Electron.*, vol. 11, no. 8, pp. 1492–1498, Jul. 2018. doi: 10.1049/iet-pel.2017.0762.

[22] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 902–913, Nov. 2010. doi: 10.1109/TEMC.2010.2064169.

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