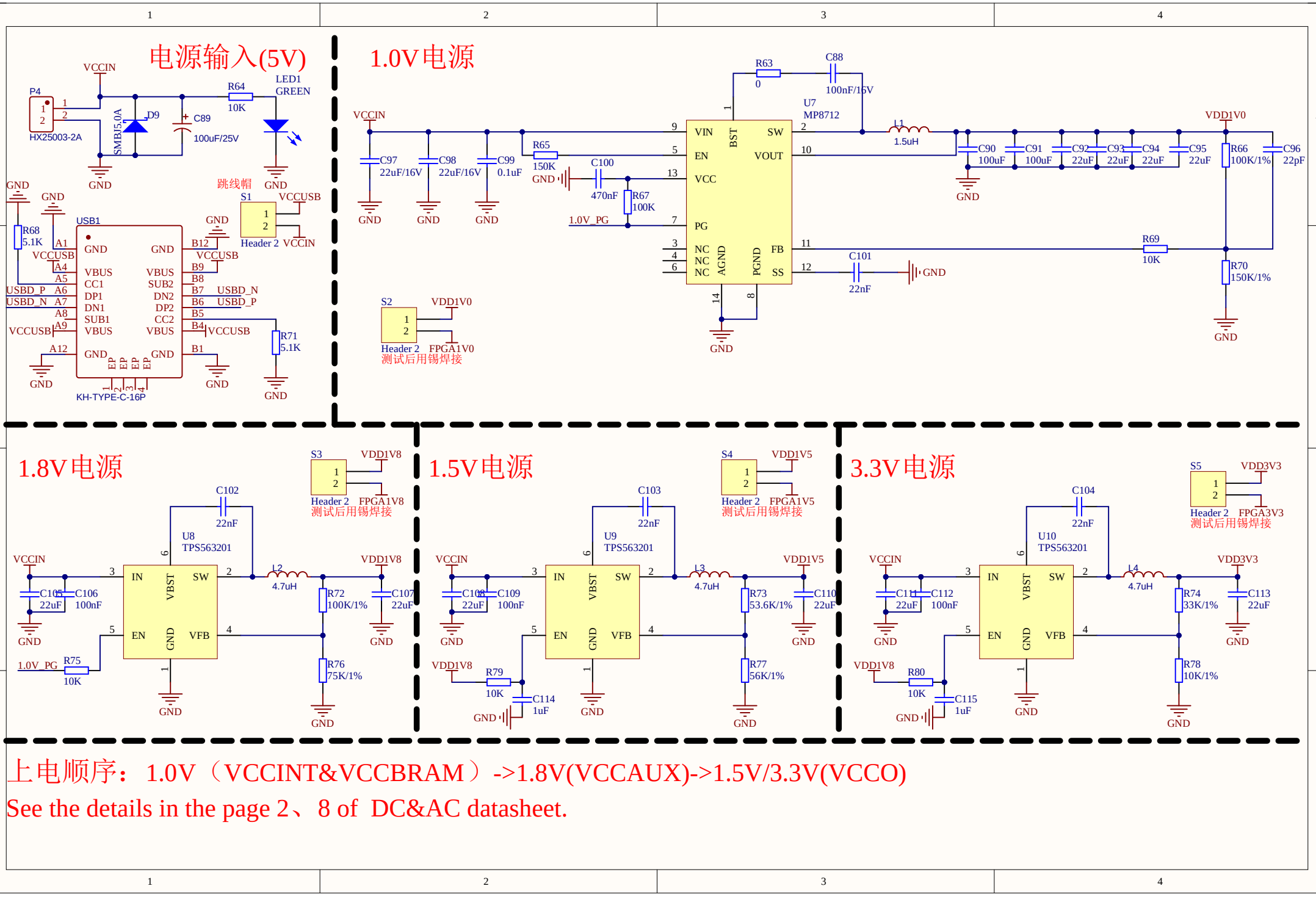
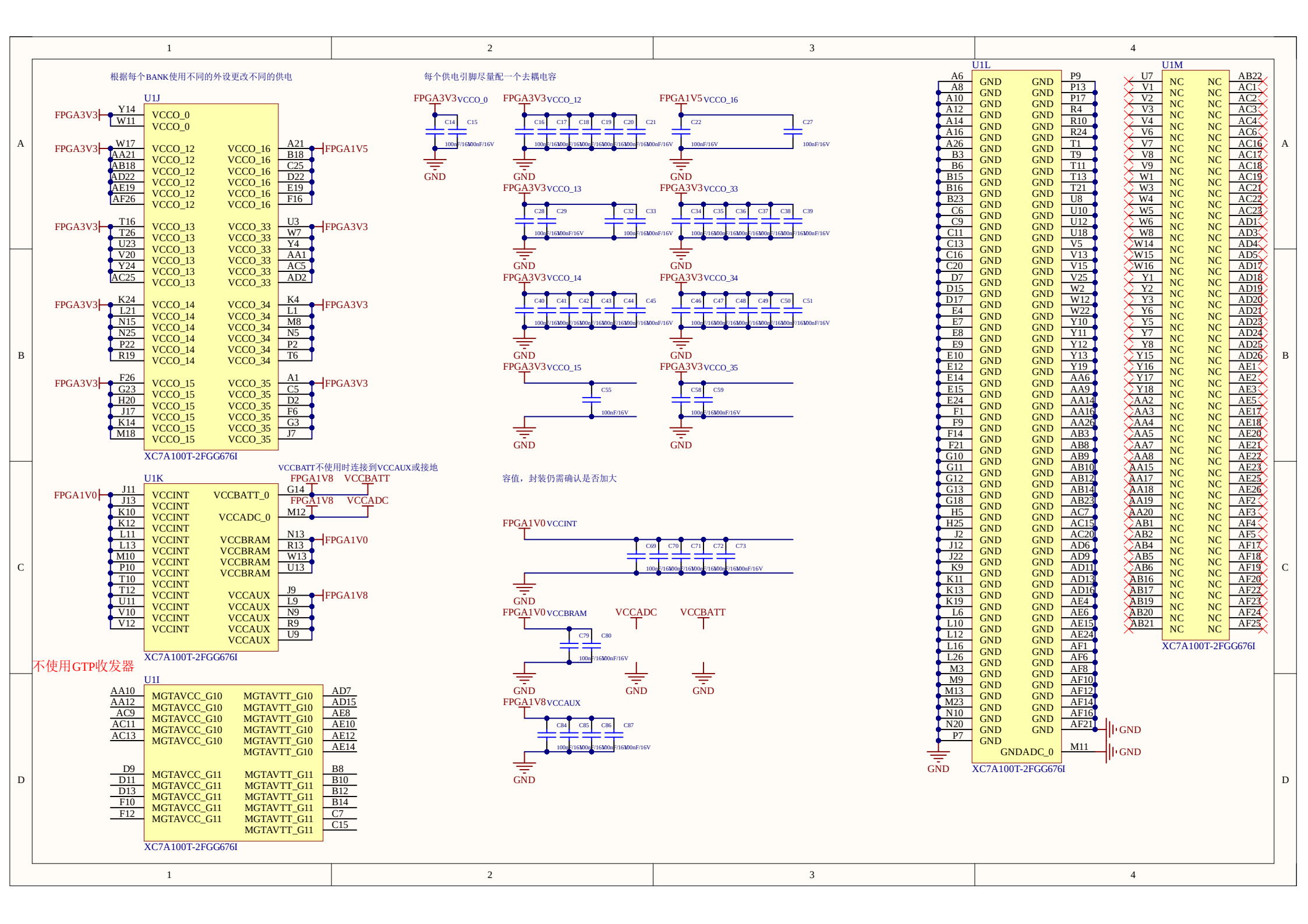
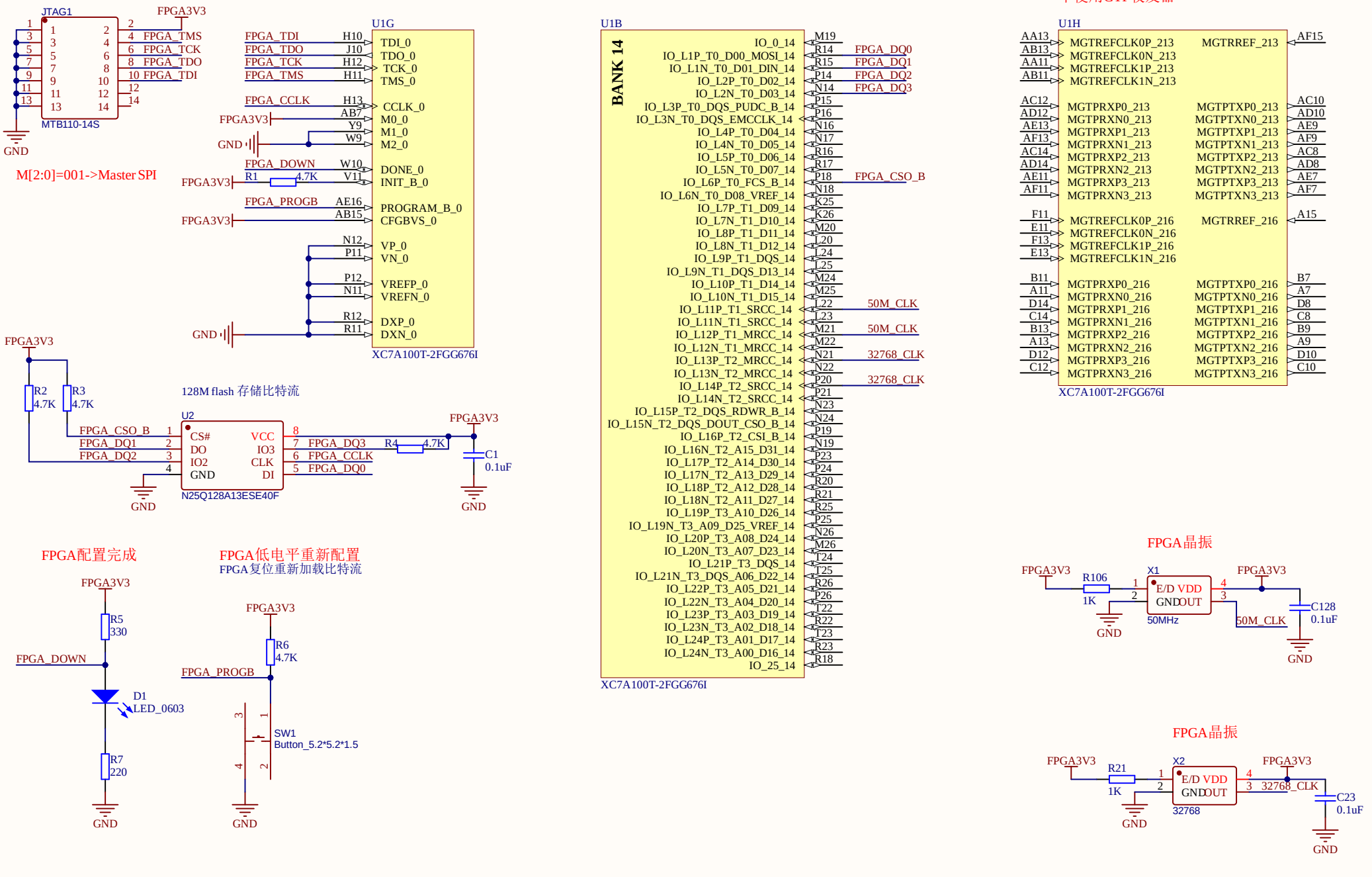

电源输入(5V)
VCCIN
P4
HX25003-2A
SMBJ5.0A
D9
C89
100uF/25V
R64
10K
LED1
GREEN
GND
跳线帽
S1
VCCUSB
Header 2
USB1
KH-TYPE-C-16P
R68
5.1K
R71
5.1K
USBD_P
USBD_N
1.0V电源
R63
0
C88
100nF/16V
U7
MP8712
VIN
EN
VCC
PG
NC
AGND
PGND
BST
SW
VOUT
FB
SS
L1
1.5uH
C97
22uF/16V
C98
22uF/16V
C99
0.1uF
R65
150K
C100
470nF
R67
100K
1.0V_PG
C90
100uF
C91
100uF
C92
22uF
C93
22uF
C94
22uF
C95
22uF
C96
22pF
R66
100K/1%
R69
10K
R70
150K/1%
C101
22nF
VDD1V0
S2
Header 2
FPGA1V0
测试后用锡焊接
1.8V电源
U8
TPS563201
C102
22nF
L2
4.7uH
R72
100K/1%
R76
75K/1%
R75
10K
C105
22uF
C106
100nF
C107
22uF
S3
VDD1V8
FPGA1V8
1.5V电源
U9
TPS563201
C103
22nF
L3
4.7uH
R73
53.6K/1%
R77
56K/1%
R79
10K
C114
1uF
C108
22uF
C109
100nF
C110
22uF
S4
VDD1V5
FPGA1V5
3.3V电源
U10
TPS563201
C104
22nF
L4
4.7uH
R74
33K/1%
R78
10K/1%
R80
10K
C115
1uF
C111
22uF
C112
100nF
C113
22uF
S5
VDD3V3
FPGA3V3
上电顺序：1.0V（VCCINT&VCCBRAM）->1.8V(VCCAUX)->1.5V/3.3V(VCCO)
See the details in the page 2、8 of DC&AC datasheet.


根据每个BANK使用不同的外设更改不同的供电
每个供电引脚尽量配一个去耦电容
U1J
XC7A100T-2FGG676I
VCCBATT不使用时连接到VCCAUX或接地
U1K
XC7A100T-2FGG676I
不使用GTP收发器
U1I
XC7A100T-2FGG676I
容值，封装仍需确认是否加大
U1L
XC7A100T-2FGG676I
U1M
XC7A100T-2FGG676I


JTAG1
MTB110-14S
FPGA3V3
FPGA_TMS
FPGA_TCK
FPGA_TDO
FPGA_TDI
GND
M[2:0]=001->Master SPI
U1G
FPGA_TDI H10 TDI_0
FPGA_TDO J10 TDO_0
FPGA_TCK H12 TCK_0
FPGA_TMS H11 TMS_0
FPGA_CCLK H13 CCLK_0
AB7 M0_0
Y9 M1_0
W9 M2_0
FPGA_DOWN W10 DONE_0
R1 4.7K V11 INIT_B_0
FPGA_PROGB AE16 PROGRAM_B_0
AB15 CFGBVS_0
N12 VP_0
P11 VN_0
P12 VREFP_0
N11 VREFN_0
R12 DXP_0
R11 DXN_0
XC7A100T-2FGG676I
R2 4.7K
R3 4.7K
128M flash 存储比特流
U2
FPGA_CSO_B
FPGA_DQ1
FPGA_DQ2
CS# VCC
DO IO3
IO2 CLK
GND DI
FPGA_DQ3
FPGA_CCLK
FPGA_DQ0
R4 4.7K
C1 0.1uF
N25Q128A13ESE40F
FPGA配置完成
R5 330
D1 LED_0603
R7 220
FPGA低电平重新配置
FPGA复位重新加载比特流
R6 4.7K
SW1 Button_5.2*5.2*1.5
U1B
BANK 14
IO_0_14 M19
IO_L1P_T0_D00_MOSI_14 R14 FPGA_DQ0
IO_L1N_T0_D01_DIN_14 R15 FPGA_DQ1
IO_L2P_T0_D02_14 P14 FPGA_DQ2
IO_L2N_T0_D03_14 N14 FPGA_DQ3
IO_L3P_T0_DQS_PUDC_B_14 P15
IO_L3N_T0_DQS_EMCCLK_14 P16
IO_L4P_T0_D04_14 N16
IO_L4N_T0_D05_14 N17
IO_L5P_T0_D06_14 R16
IO_L5N_T0_D07_14 R17
IO_L6P_T0_FCS_B_14 P18 FPGA_CSO_B
IO_L6N_T0_D08_VREF_14 N18
IO_L7P_T1_D09_14 K25
IO_L7N_T1_D10_14 K26
IO_L8P_T1_D11_14 M20
IO_L8N_T1_D12_14 L20
IO_L9P_T1_DQS_14 L24
IO_L9N_T1_DQS_D13_14 L25
IO_L10P_T1_D14_14 M24
IO_L10N_T1_D15_14 M25
IO_L11P_T1_SRCC_14 L22 50M_CLK
IO_L11N_T1_SRCC_14 L23
IO_L12P_T1_MRCC_14 M21 50M_CLK
IO_L12N_T1_MRCC_14 M22
IO_L13P_T2_MRCC_14 N21 32768_CLK
IO_L13N_T2_MRCC_14 N22
IO_L14P_T2_SRCC_14 P20 32768_CLK
IO_L14N_T2_SRCC_14 P21
IO_L15P_T2_DQS_RDWR_B_14 N23
IO_L15N_T2_DQS_DOUT_CSO_B_14 N24
IO_L16P_T2_CSI_B_14 P19
IO_L16N_T2_A15_D31_14 N19
IO_L17P_T2_A14_D30_14 P23
IO_L17N_T2_A13_D29_14 P24
IO_L18P_T2_A12_D28_14 R20
IO_L18N_T2_A11_D27_14 R21
IO_L19P_T3_A10_D26_14 R25
IO_L19N_T3_A09_D25_VREF_14 P25
IO_L20P_T3_A08_D24_14 N26
IO_L20N_T3_A07_D23_14 M26
IO_L21P_T3_DQS_14 T24
IO_L21N_T3_DQS_A06_D22_14 T25
IO_L22P_T3_A05_D21_14 R26
IO_L22N_T3_A04_D20_14 P26
IO_L23P_T3_A03_D19_14 T22
IO_L23N_T3_A02_D18_14 R22
IO_L24P_T3_A01_D17_14 T23
IO_L24N_T3_A00_D16_14 R23
IO_25_14 R18
XC7A100T-2FGG676I
不使用GTP收发器
U1H
MGTREFCLK0P_213 MGTRREF_213
MGTREFCLK0N_213
MGTREFCLK1P_213
MGTREFCLK1N_213
MGTPRXP0_213 MGTPTXP0_213
MGTPRXN0_213 MGTPTXN0_213
MGTPRXP1_213 MGTPTXP1_213
MGTPRXN1_213 MGTPTXN1_213
MGTPRXP2_213 MGTPTXP2_213
MGTPRXN2_213 MGTPTXN2_213
MGTPRXP3_213 MGTPTXP3_213
MGTPRXN3_213 MGTPTXN3_213
MGTREFCLK0P_216 MGTRREF_216
MGTREFCLK0N_216
MGTREFCLK1P_216
MGTREFCLK1N_216
MGTPRXP0_216 MGTPTXP0_216
MGTPRXN0_216 MGTPTXN0_216
MGTPRXP1_216 MGTPTXP1_216
MGTPRXN1_216 MGTPTXN1_216
MGTPRXP2_216 MGTPTXP2_216
MGTPRXN2_216 MGTPTXN2_216
MGTPRXP3_216 MGTPTXP3_216
MGTPRXN3_216 MGTPTXN3_216
XC7A100T-2FGG676I
FPGA晶振
R106 1K
X1 E/D VDD GNDOUT
50MHz
C128 0.1uF
FPGA晶振
R21 1K
X2 E/D VDD GNDOUT
32768
C23 0.1uF

BANK13、15全部连接软核CPU的外设

软核CPU拥有3组x16个通用GPIO

数据存储flash
128M flash 存储CPU程序

U1A

BANK 13

IO_0_13	U24	ETH1_TXD0
IO_L1P_T0_13	U25	ETH1_TXD1
IO_L1N_T0_13	U26	ETH1_TXEN
IO_L2P_T0_13	V26	ETH1_RXD0
IO_L2N_T0_13	W26	ETH1_RXD1
IO_L3P_T0_DQS_13	AB26	ETH1_RXER
IO_L3N_T0_DQS_13	AC26	ETH1_CRS_DV
IO_L4P_T0_13	W25	ETH_nRST
IO_L4N_T0_13	Y26	ETH_MDC
IO_L5P_T0_13	Y25	ETH_MDIO
IO_L5N_T0_13	AA25	GPIO15
IO_L6P_T0_13	V24	
IO_L6N_T0_VREF_13	W24	
IO_L7P_T1_13	AA24	
IO_L7N_T1_13	AB25	GPIO14
IO_L8P_T1_13	AA22	GPIO10
IO_L8N_T1_13	AA23	GPIO11
IO_L9P_T1_DQS_13	AB24	GPIO13
IO_L9N_T1_DQS_13	AC24	GPIO12
IO_L10P_T1_13	V23	
IO_L10N_T1_13	W23	
IO_L11P_T1_SRCC_13	Y22	
IO_L11N_T1_SRCC_13	Y23	
IO_L12P_T1_MRCC_13	U22	ETH1_TX_CLK
IO_L12N_T1_MRCC_13	V22	
IO_L13P_T2_MRCC_13	U21	
IO_L13N_T2_MRCC_13	V21	
IO_L14P_T2_SRCC_13	W21	
IO_L14N_T2_SRCC_13	Y21	GPIO9
IO_L15P_T2_DQS_13	T20	
IO_L15N_T2_DQS_13	U20	
IO_L16P_T2_13	W20	
IO_L16N_T2_13	Y20	GPIO8
IO_L17P_T2_13	T19	
IO_L17N_T2_13	U19	
IO_L18P_T2_13	V19	
IO_L18N_T2_13	W19	GPIO7
IO_L19P_T3_13	V18	
IO_L19N_T3_VREF_13	W18	GPIO6
IO_L20P_T3_13	T14	
IO_L20N_T3_13	T15	
IO_L21P_T3_DQS_13	T17	
IO_L21N_T3_DQS_13	T18	
IO_L22P_T3_13	U15	
IO_L22N_T3_13	U16	
IO_L23P_T3_13	U14	
IO_L23N_T3_13	V14	
IO_L24P_T3_13	Y16	
IO_L24N_T3_13	V17	
IO_25_13	U17	

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U1C

BANK 15

IO_0_15	K18	FLASH_CS
IO_L1P_T0_AD0P_15	K15	FLASH_DO
IO_L1N_T0_AD0N_15	J16	FLASH_IO2
IO_L2P_T0_AD8P_15	J14	FLASH_IO3
IO_L2N_T0_AD8N_15	J15	FLASH_CLK
IO_L3P_T0_DQS_AD1P_15	K16	FLASH_DI
IO_L3N_T0_DQS_AD1N_15	K17	
IO_L4P_T0_15	M14	UART_RX1
IO_L4N_T0_15	L14	UART_TX1
IO_L5P_T0_AD9P_15	M15	UART_RX2
IO_L5N_T0_AD9N_15	L15	UART_TX2
IO_L6P_T0_15	M16	CPU_JTAG_TCK
IO_L6N_T0_VREF_15	M17	CPU_JTAG_TDO
IO_L7P_T1_AD2P_15	J19	CPU_JTAG_TMS
IO_L7N_T1_AD2N_15	H19	CPU_JTAG_TDI
IO_L8P_T1_AD10P_15	L17	
IO_L8N_T1_AD10N_15	L18	
IO_L9P_T1_DQS_AD3P_15	K20	
IO_L9N_T1_DQS_AD3N_15	J20	
IO_L10P_T1_AD11P_15	J18	
IO_L10N_T1_AD11N_15	H18	
IO_L11P_T1_SRCC_15	G20	
IO_L11N_T1_SRCC_15	G21	
IO_L12P_T1_MRCC_15	K21	
IO_L12N_T1_MRCC_15	J21	
IO_L13P_T2_MRCC_15	H21	
IO_L13N_T2_MRCC_15	H22	
IO_L14P_T2_SRCC_15	J23	
IO_L14N_T2_SRCC_15	H23	
IO_L15P_T2_DQS_15	G22	
IO_L15N_T2_DQS_ADV_B_15	F22	
IO_L16P_T2_A28_15	J24	
IO_L16N_T2_A27_15	H24	
IO_L17P_T2_A26_15	F23	
IO_L17N_T2_A25_15	E23	
IO_L18P_T2_A24_15	K22	
IO_L18N_T2_A23_15	K23	
IO_L19P_T3_A22_15	G24	
IO_L19N_T3_A21_VREF_15	F24	
IO_L20P_T3_A20_15	E25	ck1
IO_L20N_T3_A19_15	D25	
IO_L21P_T3_DQS_15	E26	ck2
IO_L21N_T3_DQS_A18_15	D26	ck3
IO_L22P_T3_A17_15	H26	
IO_L22N_T3_A16_15	G26	ck4
IO_L23P_T3_FOE_B_15	G25	
IO_L23N_T3_FWE_B_15	F25	ck5
IO_L24P_T3_RS1_15	J25	
IO_L24N_T3_RS0_15	J26	
IO_25_15	L19	

XC7A100T-2FGG676I

PA0-15

T1 T2 TestPin TestPin

R14 1K
R15 1K

U4 N25Q128A13ESE40F

FPGA3V3
FLASH_CS 1 — CS# VCC 8 FPGA3V3
FLASH_DO 2 — DO IO3 7 FLASH_IO3
FLASH_IO2 3 — IO2 CLK 6 FLASH_CLK
4 — GND DI 5 FLASH_DI
GND

USB-串口

U5 CH340E

USBD_P 1 — UD+ V3 10 FPGA3V3
USBD_N 2 — UD- RXD 9 UART_RX1
3 — GND TXD 8 UART_TX1
4 — RTS# VCC 7 FPGA3V3
5 — CTS# TNOW 6
C7 0.1uF
GND

软核CPU的GPIO

PB0-15

P2 Header 16

GPIO0	R20	1K	1
GPIO1	R22	1K	2
GPIO2	R24	1K	3
GPIO3	R26	1K	4
GPIO4	R28	1K	5
GPIO5	R30	1K	6
GPIO6	R32	1K	7
GPIO7	R34	1K	8
GPIO8	R36	1K	9
GPIO9	R38	1K	10
GPIO10	R40	1K	11
GPIO11	R42	1K	12
GPIO12	R44	1K	13
GPIO13	R46	1K	14
GPIO14	R48	1K	15
GPIO15	R50	1K	16

GND
Header 4
GND

软核CPU的调试口

CN10 5103308-1

CPU_JTAG_TCK	R16	1K	1	2	ck1
CPU_JTAG_TDO	R17	1K	3	4	ck2
CPU_JTAG_TMS	R18	1K	5	6	ck3
CPU_JTAG_TDI	R19	1K	7	8	ck4
			9	10	ck5

GND

软核CPU拥有1组百兆网口PHY接口

隔离串口

U6 IL3122-3E

VOUT5V
R52 820
C8 16pF

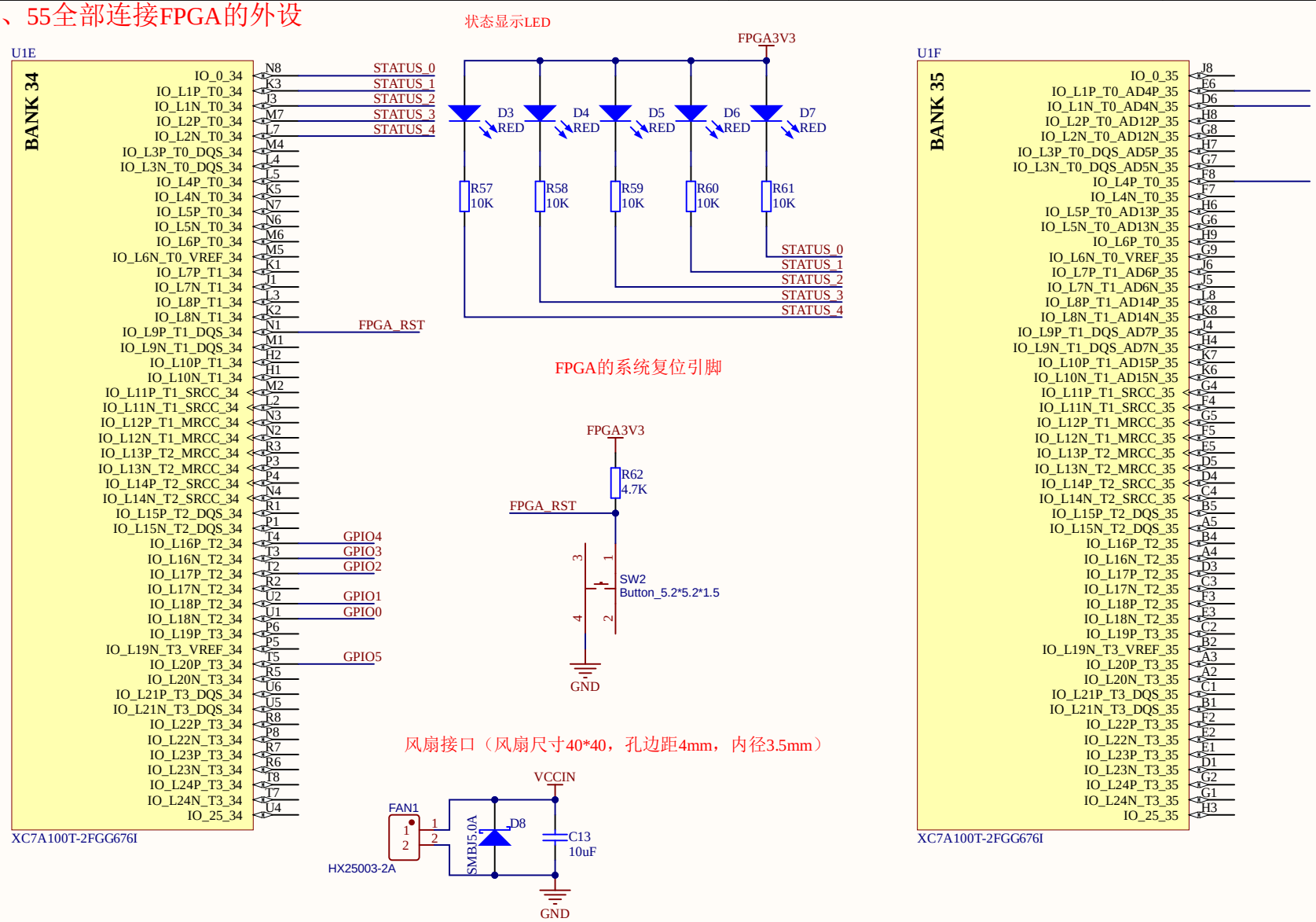
FPGA3V3	1	VDD1	VCOIL2	16	
GND	2	GND1	GND2	15	
UART_RX2 R53 0 C11 16pF GND	3	R	A	14	RE422A_R+ IGND R54 100
	4	nRE	B	13	RE422A_R-
FPGA3V3 R53 510	5	DE	Z	12	RE422A_T-
	6	VCOIL1	VDD2	11	VOUT5V
FPGA3V3 UART_TX2 R56 510 C12 16pF	7	D	Y	10	RE422A_T+
	8	NC	GND2	9	IGND

ISO1 HX25003-2A
VOUT5V
D2 SMBJ5.0A
C9 10uF
C10 0.1uF
IGND

RS1 HX25003-5A

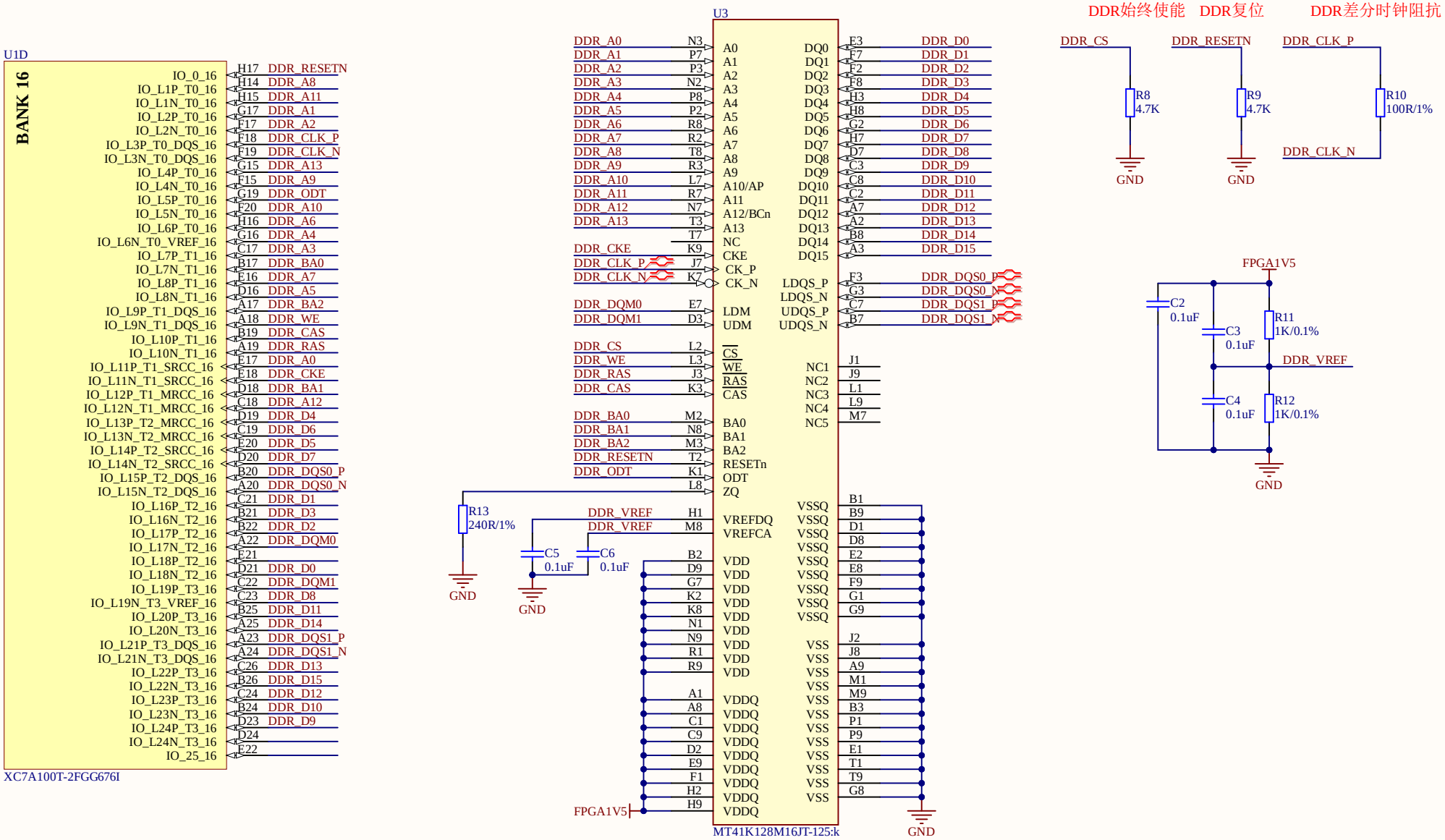
RE422A_R+	1	1
RE422A_R-	2	2
RE422A_T+	3	3
RE422A_T-	4	4
IGND	5	5

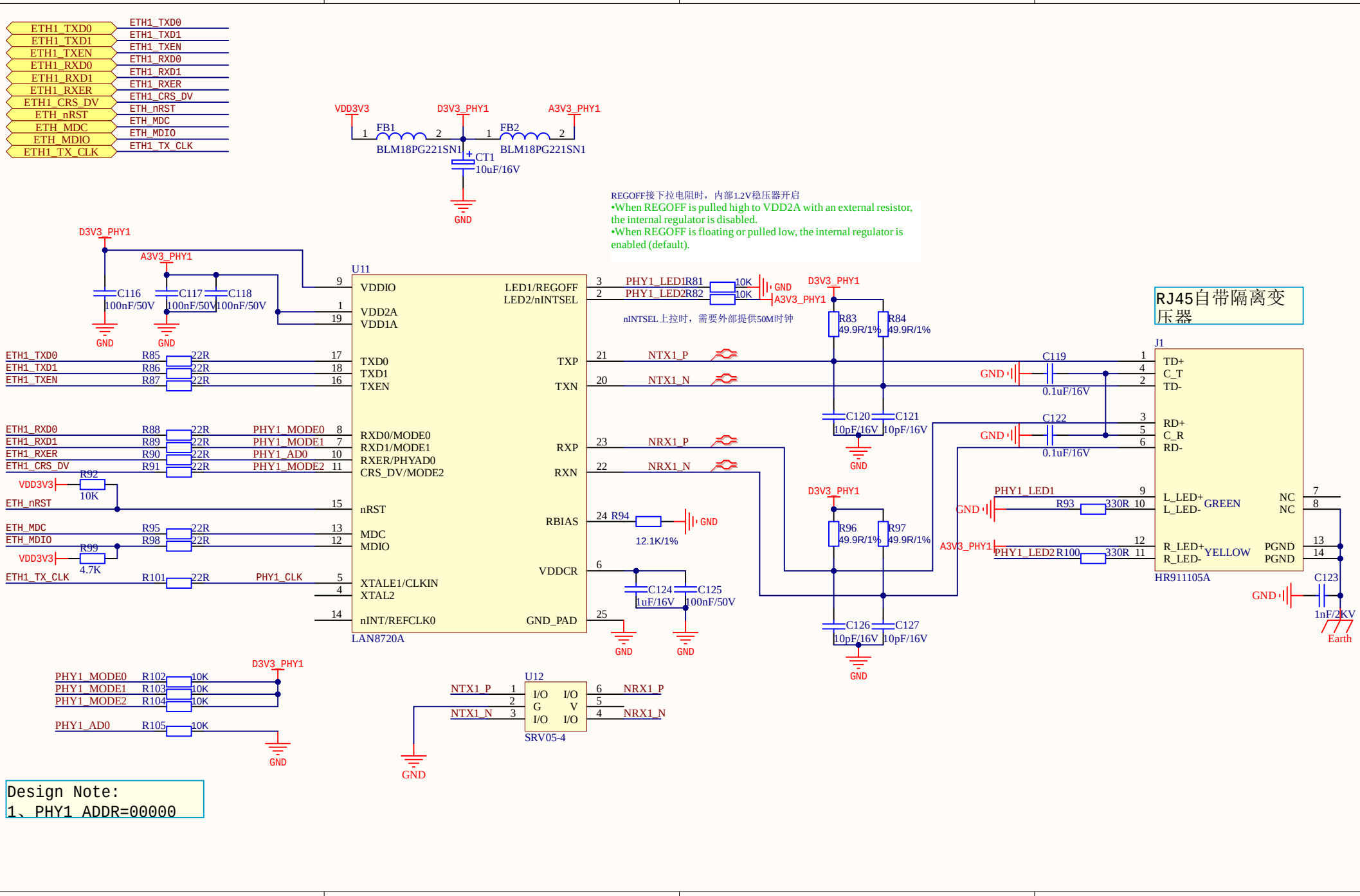
BANK34、55全部连接FPGA的外设

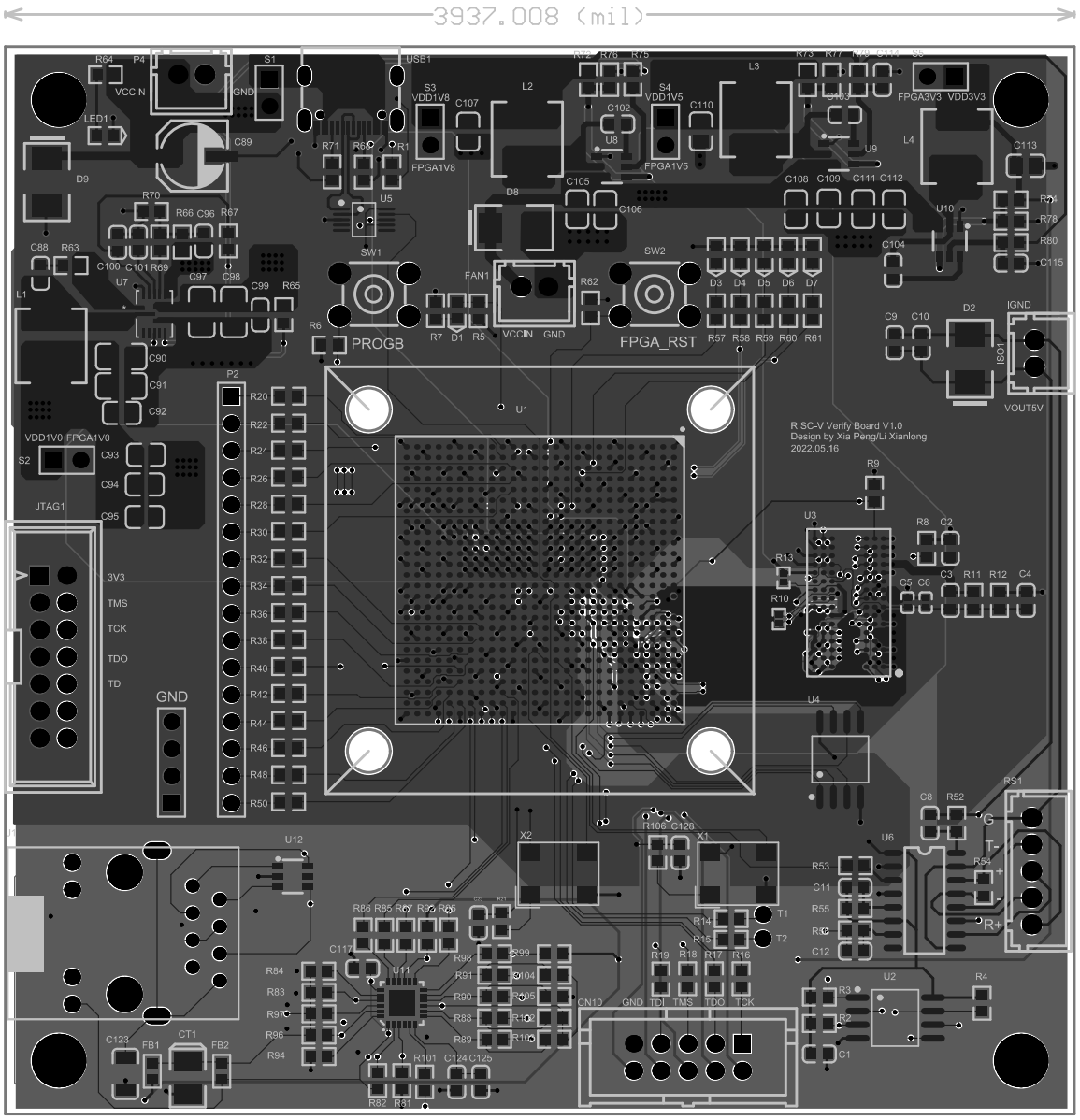


BANK16全部连接专门连接DDR3，作为软核CPU的内存

DDR三组差分线布线要注意




ETH1_TXD0
ETH1_TXD1
ETH1_TXEN
ETH1_RXD0
ETH1_RXD1
ETH1_RXER
ETH1_CRS_DV
ETH_nRST
ETH_MDC
ETH_MDIO
ETH1_TX_CLK
VDD3V3
D3V3_PHY1
A3V3_PHY1
FB1
FB2
BLM18PG221SN1
CT1
10uF/16V
GND
REGOFF接下拉电阻时，内部1.2V稳压器开启
•When REGOFF is pulled high to VDD2A with an external resistor, the internal regulator is disabled.
•When REGOFF is floating or pulled low, the internal regulator is enabled (default).
U11
VDDIO
VDD2A
VDD1A
TXD0
TXD1
TXEN
RXD0/MODE0
RXD1/MODE1
RXER/PHYAD0
CRS_DV/MODE2
nRST
MDC
MDIO
XTALE1/CLKIN
XTAL2
nINT/REFCLK0
LED1/REGOFF
LED2/nINTSEL
TXP
TXN
RXP
RXN
RBIAS
VDDCR
GND_PAD
LAN8720A
C116
C117
C118
100nF/50V
R85
R86
R87
R88
R89
R90
R91
22R
R92
10K
R99
4.7K
R95
R98
R101
PHY1_MODE0
PHY1_MODE1
PHY1_AD0
PHY1_MODE2
PHY1_CLK
R94
12.1K/1%
C124
C125
1uF/16V
R81
R82
PHY1_LED1
PHY1_LED2
nINTSEL上拉时，需要外部提供50M时钟
NTX1_P
NTX1_N
NRX1_P
NRX1_N
R83
R84
49.9R/1%
C120
C121
10pF/16V
C126
C127
R96
R97
C119
C122
0.1uF/16V
J1
TD+
C_T
TD-
RD+
C_R
RD-
L_LED+
L_LED-
GREEN
R_LED+
R_LED-
YELLOW
NC
PGND
HR911105A
R93
R100
330R
C123
1nF/2KV
Earth
RJ45自带隔离变压器
U12
I/O
G
V
SRV05-4
R102
R103
R104
R105
Design Note:
1、PHY1 ADDR=00000



层叠结构：JLC2313
外层单端50欧,5.78mil
外层差分100欧,3.49mil
内层单端50欧,5.17mil
内层差分100欧,3.52mil

注意：为了控制阻抗，高速线周围不得铺铜
TOP层PWR层在高速线上下必须铺铜

Board Stack Report